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Thermally and Electrically Addressed Dye Switching LCDs

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The thermally and electrically induced pleochroic dye switching effect in smectic A liquid crystal host is described. This phenomena provides inherent display memory, and thus can be multiplexed virtually without limitation. LCDs utilizing this effect have good contrast and legibility. Actual devices made have demonstrated a writing rate in excess of 1000 characters per second, a contrast ratio of about 10 to 1, and a brightness above 35% of standard white. This paper includes a brief discussion on the electronic driving system and a unique thermal management technique designed to enhance the performance of the display.

INTRODUCTION

The concept of pleochroic dye switching in liquid crystal hosts was first suggested by Heilmeier *et al*[1] in 1968 as the guest host effect in nematic liquid crystals. Various modifications of this concept have been published. The nematic host can be in a twisted nematic structure, homogeneous structure, or homeotropic structure. All these devices require an external polarizer of ¼-wave plate to obtain good display contrast.[2,3]

A major step toward commercial quality display development was made in 1974 when White and Taylor[4] pointed out that by using dyes of high order parameter in a cholesteric liquid crystal host, high contrast displays could be made without external polarizers. Such a display has a high brightness and wide viewing angle that cannot be matched by field effect twist nematic devices. The White and Taylor device utilizes the electric field induced cholesteric to nematic transition in liquid crystals of positive dielectric anisotropy. In the no field mode, the dye molecules follow the helical structure of the cholesteric host and exhibit strong light absorption. In the switched "on" condition, the dye molecules are in a homeotropic nematic

host and the absorption is at a minimum. Thus, the display provides a light image against a dark background.

Recently, high order parameter and photo-stable dyes have become available. The White and Taylor device is now a viable display for many applications. However, it has a rather weak non-linear behavior in its contrast vs voltage characteristics. Multiplexing operation utilizing the inherent threshold of the device is limited to at most a few rows.[5] Large matrix addressing is successful only by adding an external non-linear element for each display pixel.[6–9]

Among various known liquid crystal electro-optic effects, the thermally induced scattering effect in smectic A phase is especially suitable for high information content display application. This effect provides inherent memory such that it has no limitation in multiplexing capability. The written scattering state can be erased very rapidly by a combined action of heating and electric field,[10] providing the rapid information rewriting capability highly desirable in practical display applications. However, the readability of the display image formed by an optical scattering effect depends somehow on the condition of the ambient illumination.

A step forward in utilizing the thermally induced electro-optic effect for display application is to incorporate pleochroic dyes in the smectic host. Due to differential light absorption as a result of orientational switching of dye molecules, the display image aesthetics are improved. The resultant device provides good image contrast and a wide viewing angle that resembles a printed page, besides the inherent memory for unlimited multiplexing and rapid rewriting capability.[11]

The thermally induced dye switching effect

The liquid crystal host used for this device has positive dielectric anisotropy and exhibits a smectic A phase followed by either a nematic phase or cholesteric phase upon heating. However, a widely quoted material such as Octyl cyanobiphenyl (C_8H_{17} -⬡-⬡- CN) does not perform well, possibly due to its wide nematic range (32–40°C). Mixtures of cyanobiphenyls that have a wide smectic and narrow nematic temperature range are utilized for better device performance. On the other hand, a smectic and cholesteric system does not necessarily require a narrow cholesteric range for good performance.

The pleochroic dyes used in the smectic A host are generally of the same classes of dyes as developed for the White and Taylor device. However, a high order parameter dye in cholesteric-nematic hosts does not necessarily exhibit high order parameter in smectic hosts. Thus, specially selected and synthesized dyes are needed to yield good optical performance. For a

neutral colored display, multi-component dye mixtures are prepared. Figure 1 shows the absorption spectrum of a typical multi-component black dye mixture that has a 0.78 order parameter from 450 to 650 nm. For most of the formulations, the dye concentration is about 1%.

The thermally induced dye switching effect is illustrated in Figure 2. Heat is applied to a layer or liquid crystal dye mixture to raise the temperature beyond its isotropic point. As the mixture cools rapidly through the nematic or cholesteric phase to the smectic phase, it can form two different textures. With a field applied, the liquid crystal host is switched to a homeotropic state during the nematic or cholesteric phase, and assumes the homeotropic smectic A texture after cooling is completed. The dye molecules in this host configuration have minimum absorption, making the material clear and indistinguishable from the surrounding. In the case of rapid cooling without the applied field, a severely distorted smectic focal conic texture is formed. The dye molecules in this host configuration absorb incoming light strongly. The material in this state is deeply colored or dark. Thus, by controlling the applied field, a light or dark state can be written in the liquid crystal dye mixture layer. Moreover, both of these states are stable after they are written. Thus, displays utilizing this electro-optical effect have inherent memory.

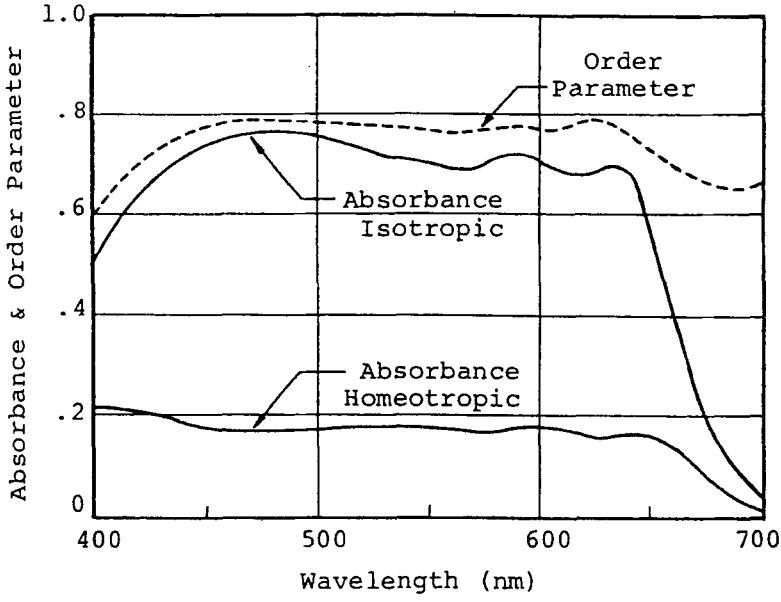

FIGURE 1 Absorption spectrum of multicomponent black dye.

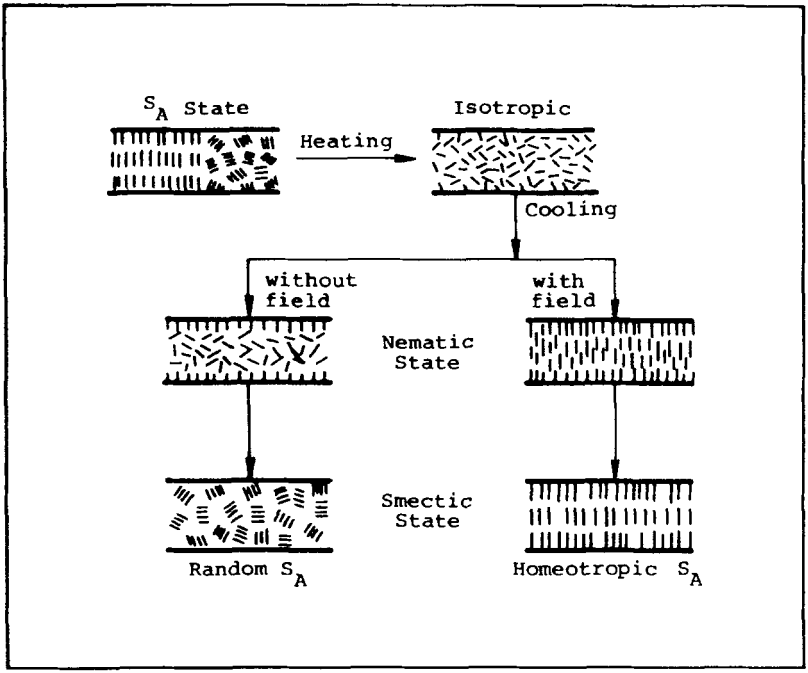

FIGURE 2 The basic E-O effect of thermally addressed display.

It is noted that during the heating period, any previously written state is erased. Thus, this electro-optical effect also provides automatic erasing during the rewriting process.

Display device construction

The construction of the display device is quite simple and conventional. The liquid crystal dye mixture is sandwiched between two substrates where the row and column electrodes are deposited. For displays having character blocks or lines separated by non-addressable gaps, the inner surface of the substrates are treated with alignment agents similar to DMOAP to provide homeotropic alignment. In displays consisting of continuously addressable pixels, no alignment layer is used.

Figure 3 shows a typical cross-section of such a device. The column plane consists of etched conventional indium tin oxide electrodes brought out to alternating column contacts. The row electrodes are typically aluminum strips 2 μm thick. The metal is sputtered in conventional fashion. Row patterning is readily achieved with conventional photolithographic meth-

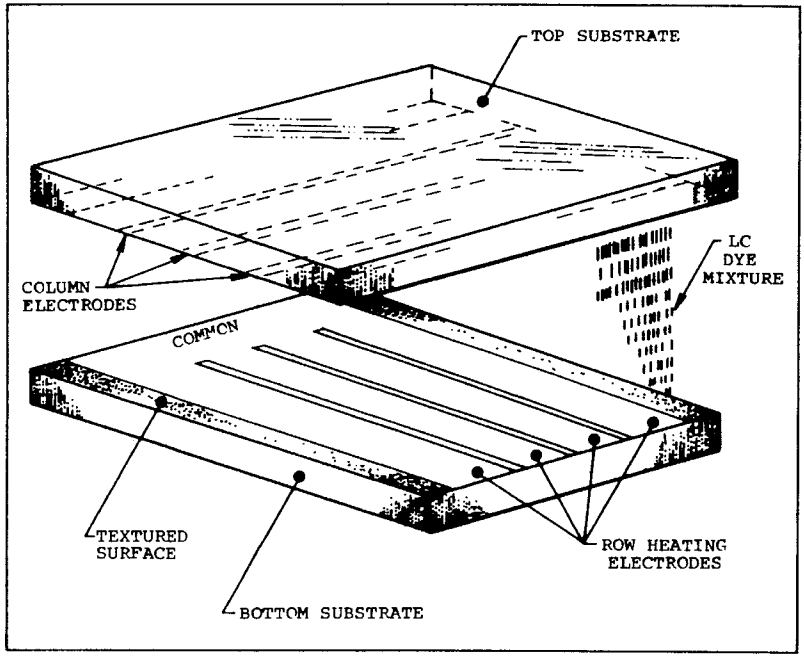

FIGURE 3 Cross-section of a thermally addressed dye switching display.

ods. The row electrodes are brought out to commons on a 1:16 basis, and to individual contacts on the alternate side of the commons.

The cell spacing has to be wide enough to ensure a good contrast ratio, typically greater than 12–14 μm. On the other hand, with cells fatter than 18–20 μm, the column voltage and the writing energy become excessively high. The optimum cell spacing is therefore 16 μm $\pm$ 2 μm.

Achieving the necessary ± 2 μm uniformity is accomplished through the use of fine precise glass fibers uniformly dispersed over the glass surface. The devices are sealed with a screened thermoplastic material that has excellent temperature and humidity resistance.

Cell filling is accomplished *via* standard single hole vacuum/pressure fill methods. Contact to the display is made *via* a flexible conductor bonded directly to the row electrode and pressure contacted to the column electrode.

The opaque Al row electrodes also act as the reflector. A specular mirror surface reflector provides a narrow viewing cone and poor legibility.

Conventional diffusing metal reflectors deposited over frosted glass surface result in too great a light loss. The approach taken is to form on the

glass surface a faceted reflector that gives an approximately 4x gain over a Lambertian reflecting surface. This reflector, in filled displays, gives a wide viewing cone (greater than 150°) with high, wide, peak brightness. The result is a bright, highly legible display resembling a printed page.

Display operation

The display is $x - y$ matrix addressed in a mode similar to those described by Hareng and LeBerre.[10] The rows are electrically connected together at one end to the ground (Figure 4). In writing the display, the rows are scanned with a voltage pulse capable of delivering a current through the addressed row. This current heats up the liquid crystal mixture adjacent to the row into the isotropic state. During the cooling period, the pixels associated with the row can be written to a colorless homeotropic state or deeply colored focal conical state by applying or not applying a voltage on the column electrodes. Thus, the display is written one row at a time. The rows can be sequentially scanned as well as randomly addressed.

The waveform of writing a character "A" is illustrated in Figure 4. Practical circuitry considerations dictate a DC driving waveform for the row. The AC column driving is essential to ensure long display life.

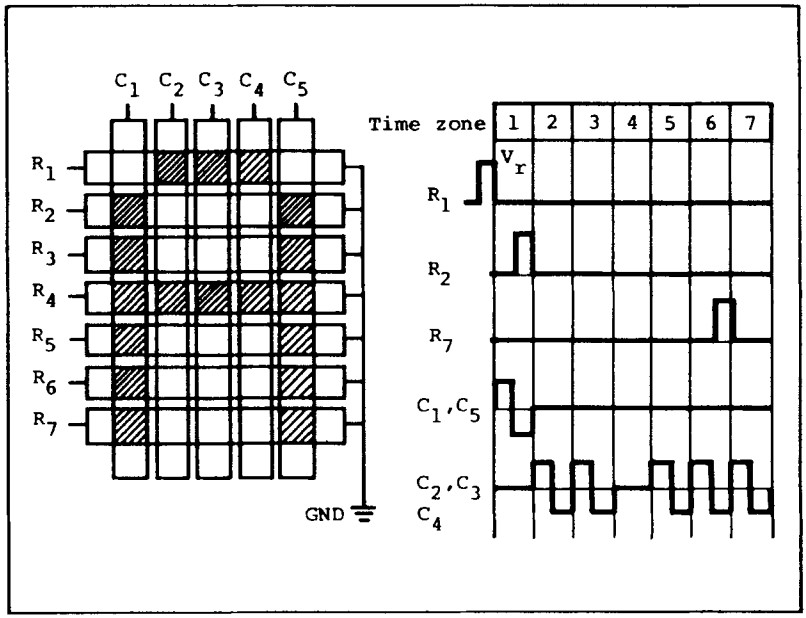

FIGURE 4 The display driving waveform.

The time required to write a row depends upon the cooling rate. The column pulse has to cover the time required for the entire liquid crystal layer over the row to cool through the nematic or cholesteric phase. With a glass substrate, this usually requires 4 to 10 msec depending on the row heating energy and the display panel temperature. Since the column voltage pulse for writing the nth row can overlap with the heating pulse on the $(n + 1)$th row, the maximum writing rate is limited by the column pulse width, i.e. at the rate of 4–10 msec per row. For displays having high thermally conductive substrates, a much faster writing rate has been observed.

Display optical performance

The contrast ratio obtained on a thermally addressed dye switching display is illustrated in Figure 5 as a function of the row heating energy density. The

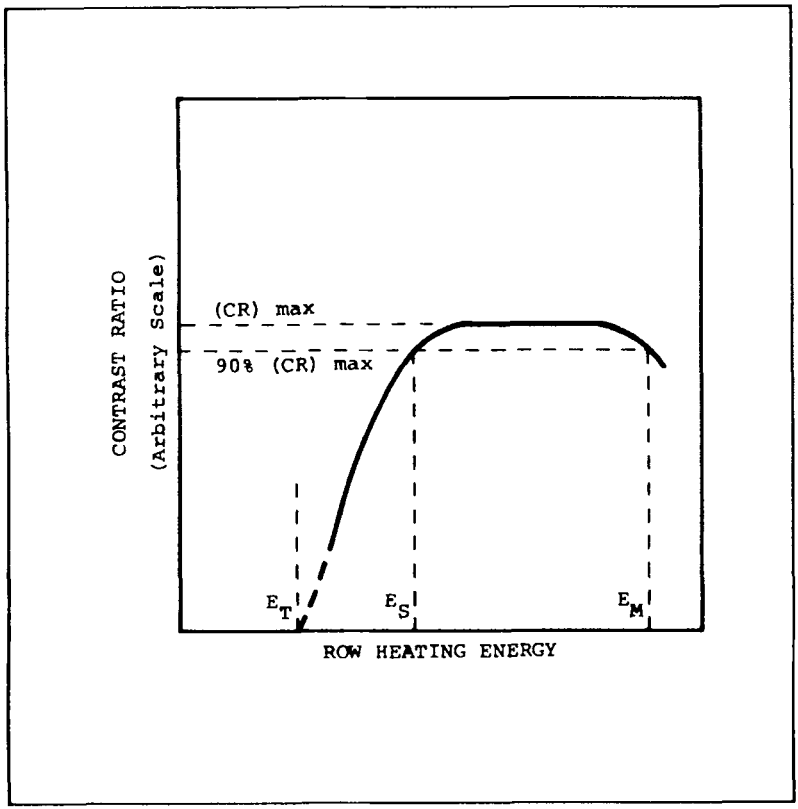

FIGURE 5 Typical display contrast ratio *vs* heating energy curve.

curve shows that a threshold energy density E_T has to be reached before observing optical contrast. The E_T value is independent of the display panel spacing. Subsequent temperature measurements, with thin film sensors fabricated on the row electrodes, indicate that E_T corresponds to the energy level where the peak row surface temperature reaches the isotropic transition point of the liquid crystal mixture. With our typical mixture developed for office equipment display applications, E_T is about 500 mJ/cm^2 at a 30°C panel temperature (Figure 6).

The display contrast has a wide saturation region from E_S to E_M. E_S is the minimum energy density required to reach saturation contrast. Its value increases with the cell spacing. Results of computer simulation on the thermal process suggest that E_S corresponds to the energy density required to heat the entire liquid crystal layer into the isotropic state. Unfortunately, column electrode temperature measurements *via* thin film sensors failed to yield accurate data to support this claim. The value of E_M is usually too

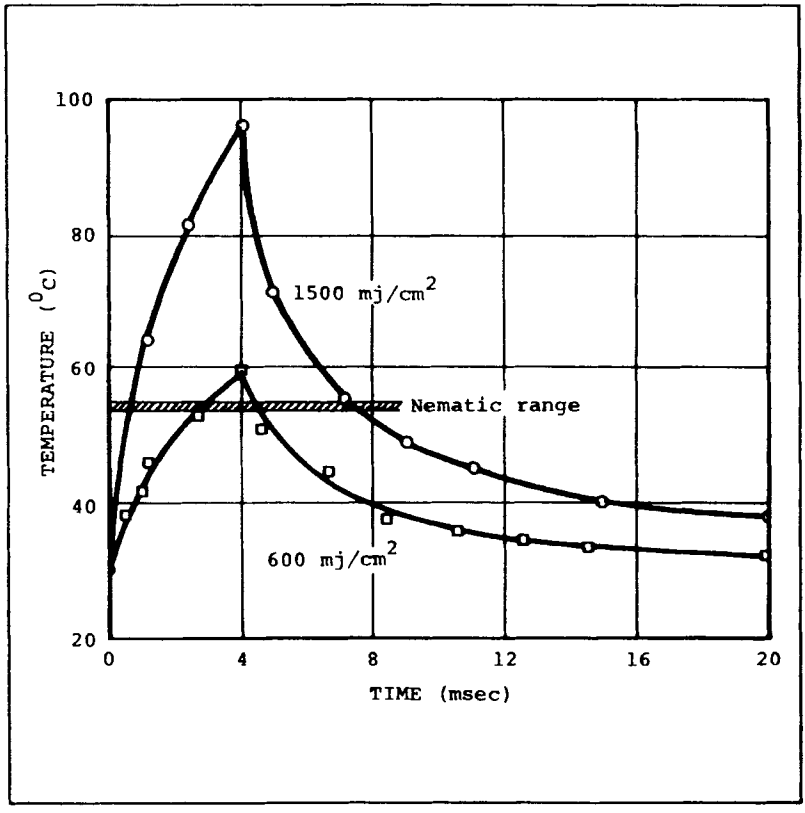

FIGURE 6 The row electrode temperature during heating and cooling.

high to be observed except with a thermal barrier layer described later.

The actual data on the saturation contrast ratio, threshold energy density E_T, and the saturation energy density E_S is shown in Figure 7.

The peak contrast ratio observed without black dye mixture exceeds 20 to 1 at 25°C. As the temperature rises, the display contrast is reduced. Figure 8 shows this relationship. All the curves should converge to the S_A to nematic or cholesteric transition temperature (54°C) at zero contrast (contrast ratio = 1).

The contrast ratio and the background brightness of a typical display is shown in Figure 9. Normally, the display is designed to have a contrast ratio of about 10, and a brightness between 35 to 40% of the standard white.

Texture study

The deeply colored state and its formation sequence have been studied extensively, *via* optical microscopy, with various cooling rates and heating

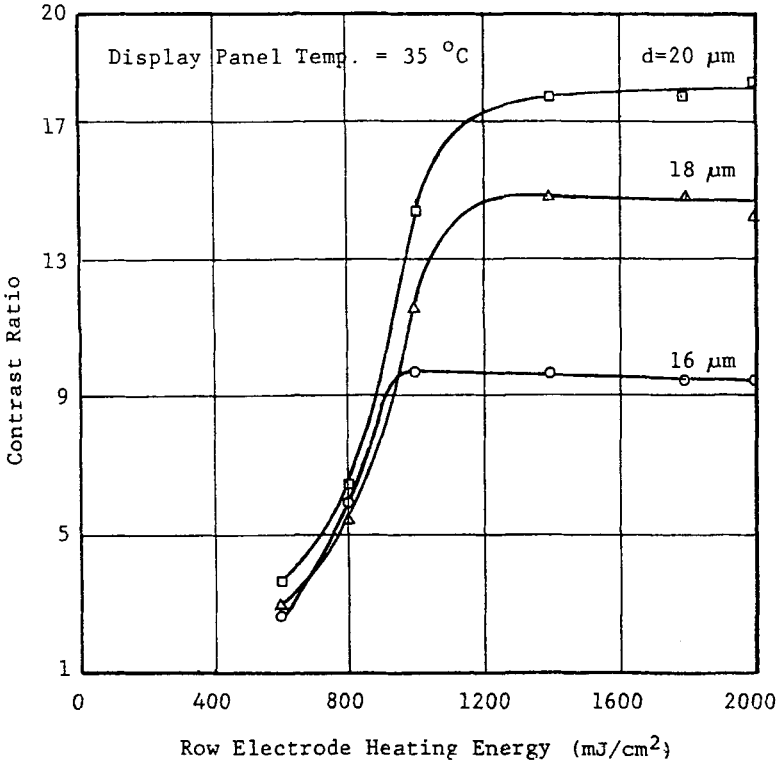

FIGURE 7 The display contrast ratio as a function of row heating energy density and cell spacing.

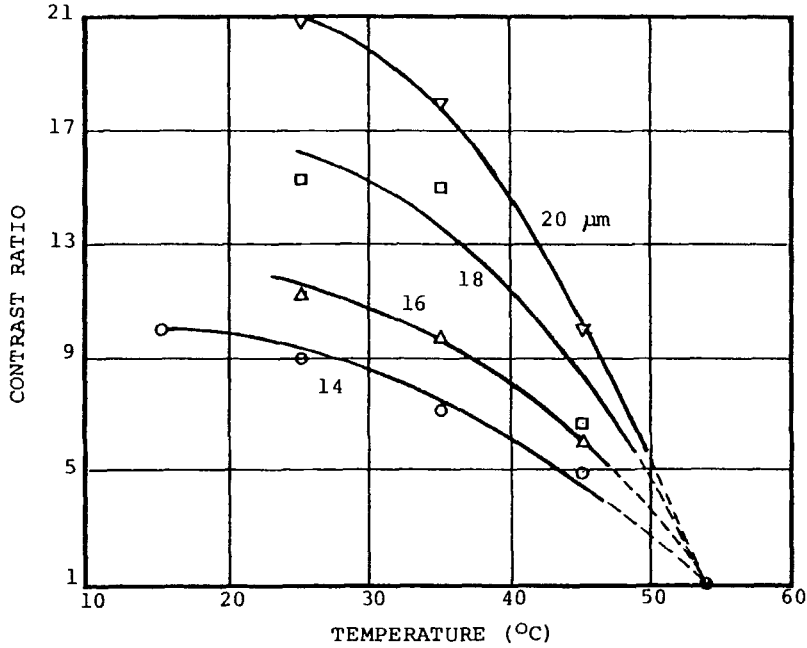

FIGURE 8 The contrast ratio at saturation heating energy.

energy densities. At the saturation contrast, the texture reveals small "grains" of about 1–3 μm size which are randomly oriented. The work "grain" is somewhat misleading since there are no sharp boundaries among individual grains. At energy density slightly above the threshold, we observe blister-like growth of grains at the row electrode surface (Figure 10). In areas where the heating is not uniform, the grains are usually arranged in a pattern which approximately follows the thermal gradient pattern (Figure 11). The honeycomb texture observed by Cladis and Torza[12] which is responsible for the light scattering effect in Kahn's laser addressed light valve[13] is not observed, presumably because a bend nematic phase structure does not exist in this device.

During transient observations of texture formation, significant material flow has been observed. Obviously, this is caused mainly by the severe thermal stress generated by excessive thermal expansion. By using video microscopy analysis of slow cooling (about 10°C per sec) experiments, we observed starburst shaped nucleation sites during the initial stage of the texture formation. Unfortunately, high speed microscopy equipment was not available to study this transient phenomena at normal cooling rates of on the order 10^4°C/sec.

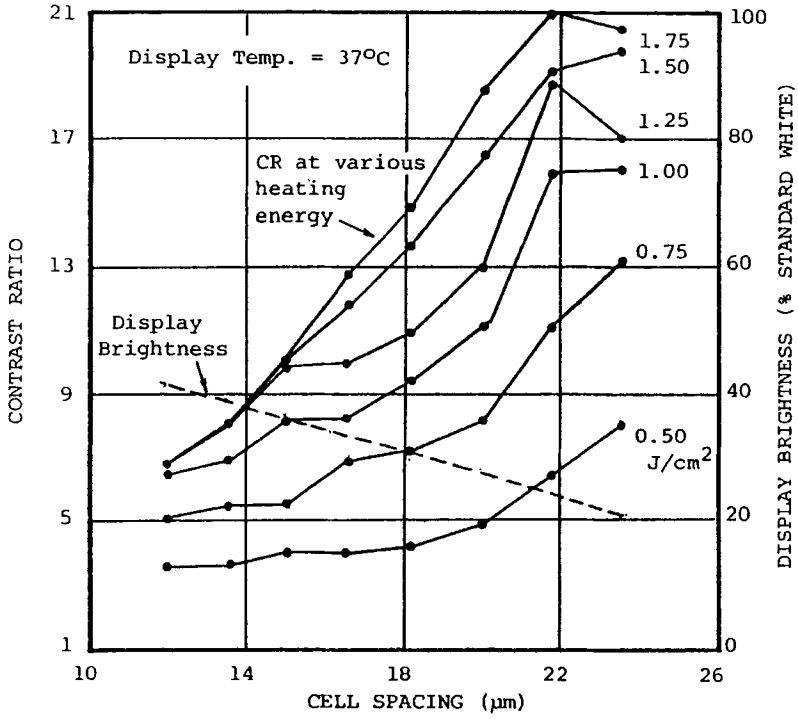

FIGURE 9 The display contrast ratio and brightness as a function of the cell spacing and the row heating energy density.

The results of texture study suggest two main mechanisms responsible for the formation of the deeply colored texture.

(1) Quenching effect due to rapid phase transition.

(2) Mechanical action generated by material flow.

It is also concluded that the dye switching effect must be a bulk effect in order to have good display contrast, where the optical scattering associated with the thermally addressed smectic device can be caused by surface texture only.

The electronic driving system

The relationship between panel spacing and the column writing voltage (V_{col}) is shown in Figure 12. The writing voltage is defined as the column voltage to attain 90% of the saturation contrast ratio. It can be seen that for 16 ± 2 μm panels, the required V_{col} is less than 25 V.

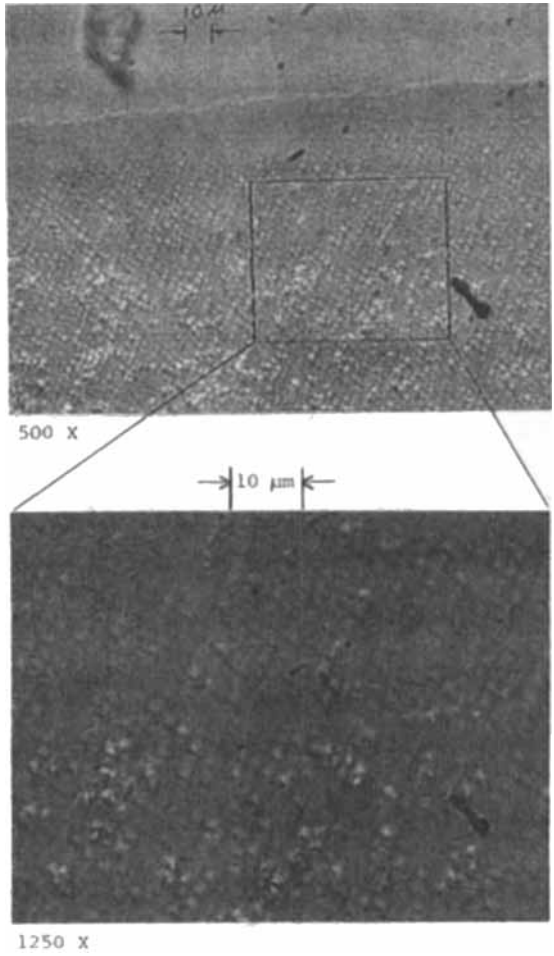

FIGURE 10 The liquid crystal texture at row heating energy slightly higher than the threshold.

The written image in the memory state can be affected, or even erased, by a column voltage much higher than the writing voltage. This effect limits the column voltage operating window which is normally limited by display crosstalk. Thus, we define the crosstalk threshold as the column voltage that causes a 10% contrast ratio reduction on the written image in the memory state.

The crosstalk threshold defined this way decreases as the pulse length of the applied voltage increases. The result is a narrower operating window.

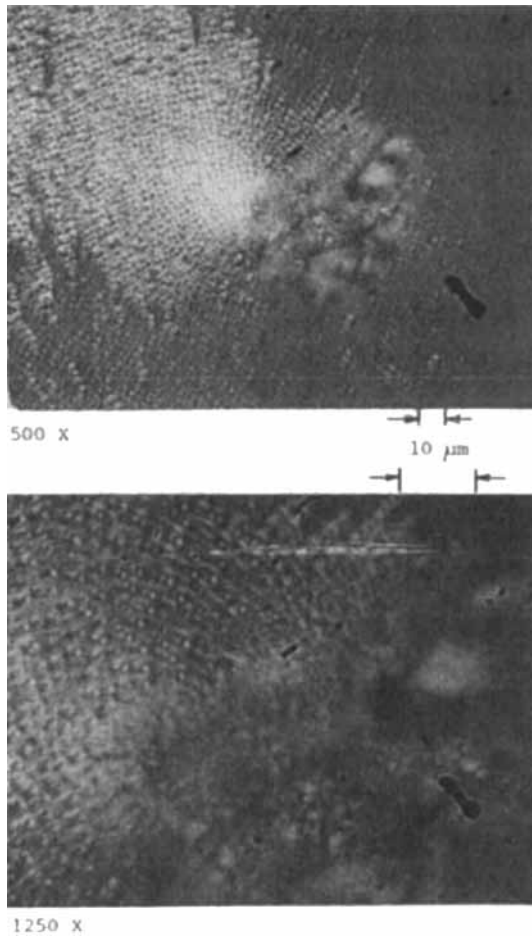

FIGURE 11 The liquid crystal texture formed around a hot spot on the row electrode. The out-of-focus large cloudy image is some confocal texture on the top glass surface where the column electrode is located.

In the worst case, on a column with no pixel in the dark state, the voltage is applied 100% of the frame time. Thus, the crosstalk threshold is measured with a 1.5 sec pulse length, which is approximately equal to the frame time. The result is also shown in Figure 12. For display panels with a spacing of about 16 μm, the column voltage operating window is very wide. This ensures a desired high multiplexing operation without the tight panel spacing control, which is critical for other types of liquid crystal displays.

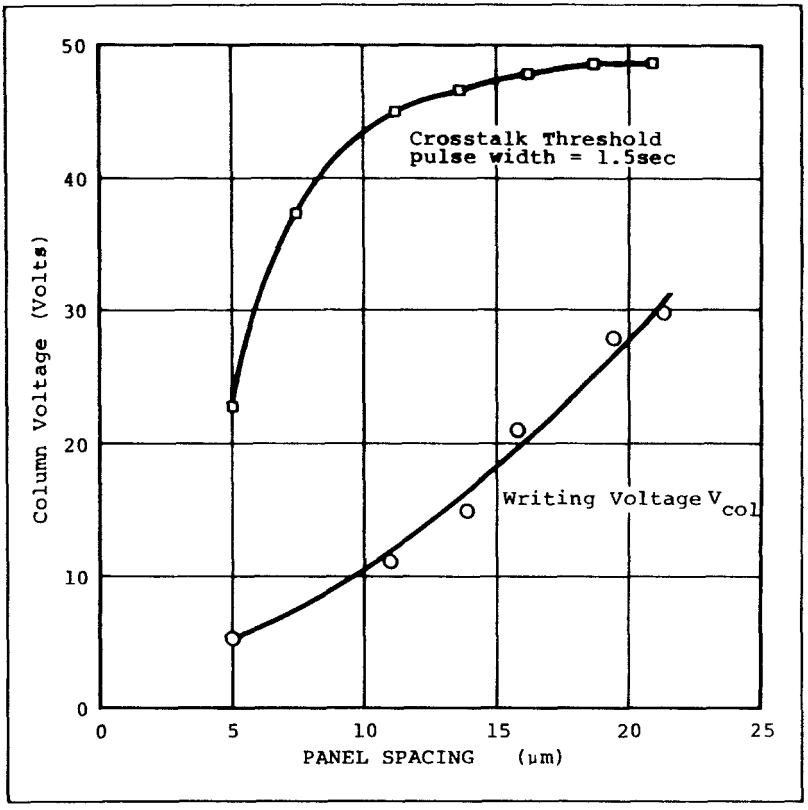

FIGURE 12 Panel spacing *vs* column voltage.

The column field is a switch field that does not require significant current. Thus, the column driving circuitry can be implemented with standard low power integrated circuit technology.

The row voltage and current requirements can be calculated from the heating energy density needed for saturation contrast ratio and from the row electrode area and its resistance. Typically, they are about 40 V and 2 A for a 6″ x 7″ display size having a pixel size of about 0.015″.

The driving waveforms are illustrated in Figure 4. As with all liquid crystal based displays, DC biasing must be held to a minimum. Thus, the column waveform has to be AC to assure long life. During the heating period, the selected row conducts current from the row power supply. This creates a DC bias across the liquid crystal cell. Fortunately, the cumulative time that a DC voltage is applied on a given row during the expected display

life span is not enough to cause serious device degradation. Moreover, an SiO_2 layer is sputtered over the row electrodes to reduce any potential residue effect due to this DC component.

Both the row drive and column drive functions have been implemented with commercial discrete drivers, as well as with custom integrated circuits.

The row driver chip consists of a 4 to 16 line decoder/driver with each of the 16 outputs capable of sinking 2 A to ground. The column driver chip is functionally a 56-bit cascadable shift register with parallel latches. The latch output is a push-pull structure capable of greater than 40 V operation. Both chips employ commonly available technologies; the row chip utilizes a standard sinker bipolar process while the column chip utilizes metal-gate CMOS technology.

Temperature compensation

Multiple, rapid writing cycles on a given row will quickly raise the liquid crystal temperature well beyond the isotropic transition point, thus rendering the display inoperative. Thus, some form of temperature compensation is needed. The most effective way to implement this function is to modulate the row heating pulse width to deliver the right amount of energy needed for satisfactory display performance. Table I shows the minimum energy density E_S and the row pulse width required for saturation display contrast. Overpowering the display does not affect the optical performance but causes an unnecessary rapid temperature rise, resulting in non-optimized operation.

TABLE I

Row pulse width modulation

Temperature of LC	Thermal energy density for Cr saturation	Row Pulse Width
25°C	1250	3.0
30°C	1000	2.4
35°C	760	1.8
40°C	550	1.33
45°C	320	0.77
	mJ/cm^2	ms

Row pulse width for 40 V; 8 Ωcell resistance, 16 μm cells, no barrier layer, 5″ × 0.015″ row.

The temperature compensation curve given in Table I can be implemented quite easily if one can measure the liquid crystal temperature. Unfortunately, this is not cost effective in physical devices. Also, the large temperature gradient and the time delay across the display substrate, prevent effective control by sensing the surface temperature outside the display panel. Thus, the approach taken is to use a software-based scheme coupled with ambient temperature sensing.

The scheme is illustrated in Figure 13. From actual liquid crystal temperature measurements by resistance sensor, we found the cooling curve to be approximately exponential. By knowing the time between subsequent heating pulses applied on a given row and the ambient temperature, the liquid crystal temperature can be calculated and the required heating pulse width can be determined. The ambient temperature is actually the temperature of the heat sink. In our display system, a thin aluminum heat sink is attached to the back of the display to remove heat more effectively and

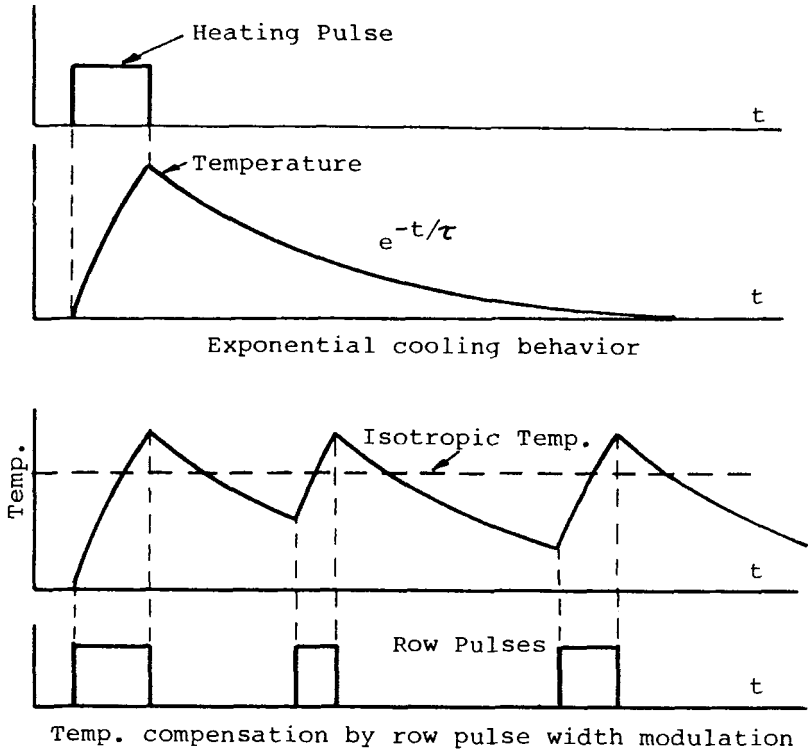

FIGURE 13 A software based temperature compensation scheme is used to enhance the performance of the thermally addressed dye switching display.

also equalize thermal gradients due to local hot spots. A thermistor sensor and an analogue to digital converter is used to provide the ambient temperature input to a microprocessor.

When a write request is generated, the microprocessor reads the ambient temperature and checks the time that the selected row was last written. If the row was written a long time ago, such that it has returned to ambient, then the full heating pulse width at that ambient will be applied to the row. If the row was recently written, the exponential cooling curve is used to calculate the proper heating pulse width factored by the current ambient temperature reading from the sensor.

This compensation scheme was implemented on a display installed in a portable terminal. The result was quite satisfactory. The Z-80A microprocessor in the terminal performed the additional task of pulse width calculation for display temperature compensation.

Thermal management

The thermally addressed dye switching display has the capability for CRT-type applications. Most of the non-TV CRT functions, such as rapid information updating, scrolling, etc. can be implemented, provided one can supply enough power and be able to remove the heat generated in the display. Therefore, good thermal management design is the key to enhance the display performance to satisfy demands required as a CRT replacement. The temperature compensation scheme described above is one form of thermal management. Other techniques include the use of proper heat sinks, cooling devices, and the thermal barrier layer.

The heat sink is a metal plate with large surface area that keeps good thermal contact with the display. Besides serving as a more efficient heat removal means, it also acts as a temperature equalizer that eliminates local hot spots due to excessive local selective rewriting.

Computer simulation of the thermal process during writing indicated that a large percentage of the applied heating energy served to heat the glass substrate rather than the liquid crystal mixture. In fact, the thermal conductivity of the glass is many times greater than that of the liquid crystal, resulting in inefficient heating process. Displays have been fabricated, therefore, with a layer of polymer (*e.g.* polyimide) between the metallic row electrodes and the glass substrate. Indeed, this thermal barrier layer improves the heating efficiency. Figure 14 shows the effect on saturation energy density E_S required to achieve full contrast. The results confirm the computer model and show that energy levels are reduced by 60% with this approach. Complete 288 × 360 matrix displays of 6″ × 7″ size have been fabricated with thermal barrier layers. The devices perform as predicted,

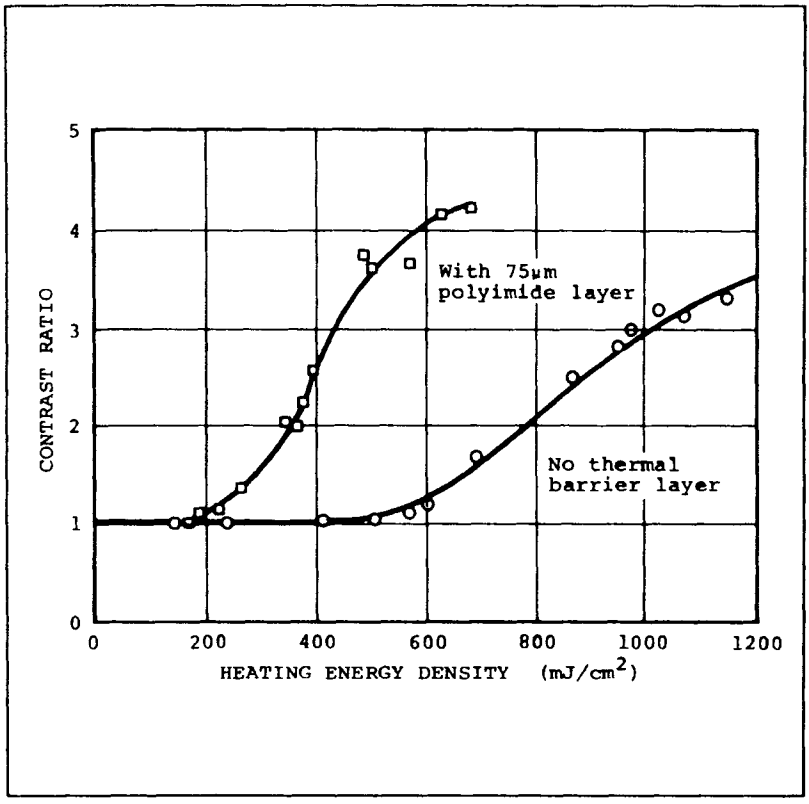

FIGURE 14 Effect of thermal barrier layer on heating.

but the quality of the surface reflector at this stage of development is poorer than the displays fabricated on plain glass substrates.

The energy density required to achieve saturation contrast is listed in Table I. If we use a fixed column pulse width of 5 msec, the writing rate in characters/sec can be calculated. Since row and column pulses are applied sequentially, only the longest time period is restrictive. A 288 row display can therefore be written in 288 × 5 msec = 1.4 seconds, giving no power or temperature limitations. Thus 1200 characters (a 288 × 360 matrix, 5 × 7 character) can be written in 1.4 sec, giving an approximate 900 characters/sec write rate.

In practice, the power level supplied to the system can also serve as a restriction on write rate when the display is addressed in a continuous scroll mode. Table II details power levels at different continuous write rates assuming that the display equilibrates at approximately 40°C.

TABLE II

Power *vs* Write Rate at 40°C panel temperature; 550 mJ/cm² thermal energy density, 1200 character panel, 6″ × 7″ overall area; 0.015″ pixel

Write rate	Average power no barrier layer	Average power with barrier layer
1000	64	26
750	48	19
500	32	13
250	16	6
100	8	3
character/sec	watts	watts

A third restriction on the write rate is the ability to remove the heat generated in the display. Figure 15 shows the heat dissipation of a convecting surface in still air as a function of the display panel temperature rise. If we again assume that the display equilibrates at 40°C (Δt = 15°C), the power dissipation with two convecting surfaces is 50 mW/cm². This number gives a total heat removal capability of 13.5 watts for a 6″ × 7″ size display. From Table II it is seen that a display with a thermal barrier layer can be written continuously at 500 characters/sec rate. With a proper heat sink and forced air cooling, continuous writing at 1000 characters/sec can be achieved.

Devices fabricated

Three formats have been utilized as shown:

A. 240 characters (48 × 240) with 0.020″ pixel in 6″ × 2.25″ size
B. 1200 characters (288 × 360) with 0.015″ pixel in 6″ × 7″ size
C. 3600 characters (512 × 576) with 0.010″ pixel in 6″ × 7″ size

Device A was successfully routinely fabricated without defects; Device B has been fabricated with no defects (see Figure 16). Device C, which contains nearly ⅓ million pixels, represented a more difficult problem in avoiding scratches in the ITO electrodes and open electrode contacts. The level of perfection is illustrated in Figure 17.

Optical performance on these devices is defined in terms of photopic contrast ratio *CR* and background brightness *B* (as pct of standard white), both values measured perpendicular to the surface in daylight fluorescent light ambient. The *CR* and *B* achieved are functions of ambient temperature and of the energy density supplied. Very high *CR* values are

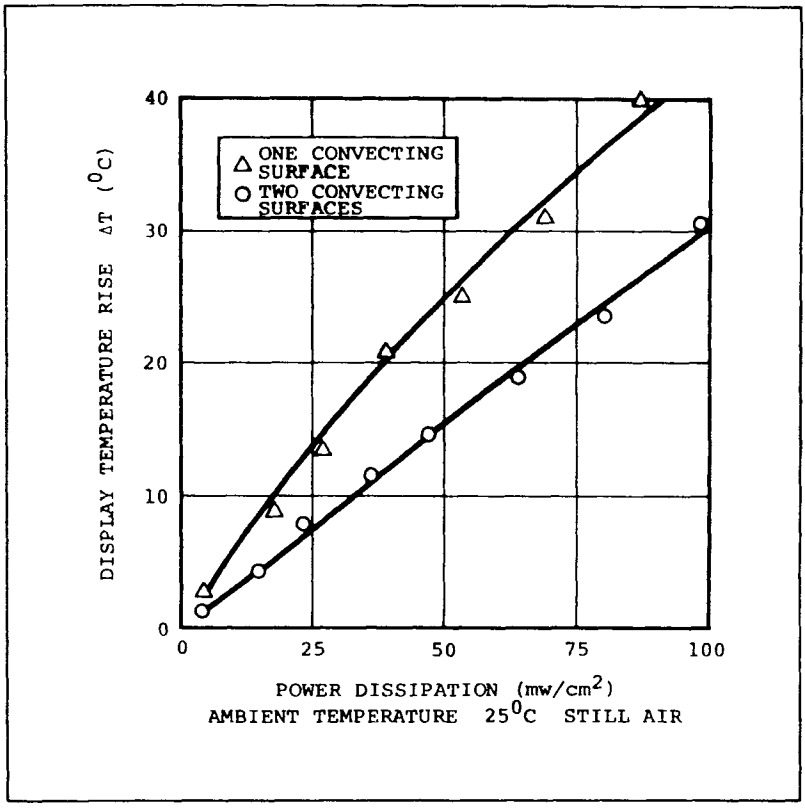

FIGURE 15 Equilibrium temperature rise at a given power input.

achievable (20:1) in thicker cells (20 μm); however, this increases the writing power and decreases the display brightness, and we therefore restrict the spacing about 16 μm.

CONCLUSION

The basic principle of pleochroic dye switching in smectic A liquid crystals using a thermal address mode is described. The advantages of this approach for fabricating multi-character flat panel displays are as follows:

(1) Very high inherent multiplexability arising out of the large threshold difference between the voltage threshold in the intermediate phase (nematic or cholesteric) vs the smectic state.
(2) The good viewing cone and image legibility arising out of the use of pleochroic dyes in this application compared to the use of scattering state.

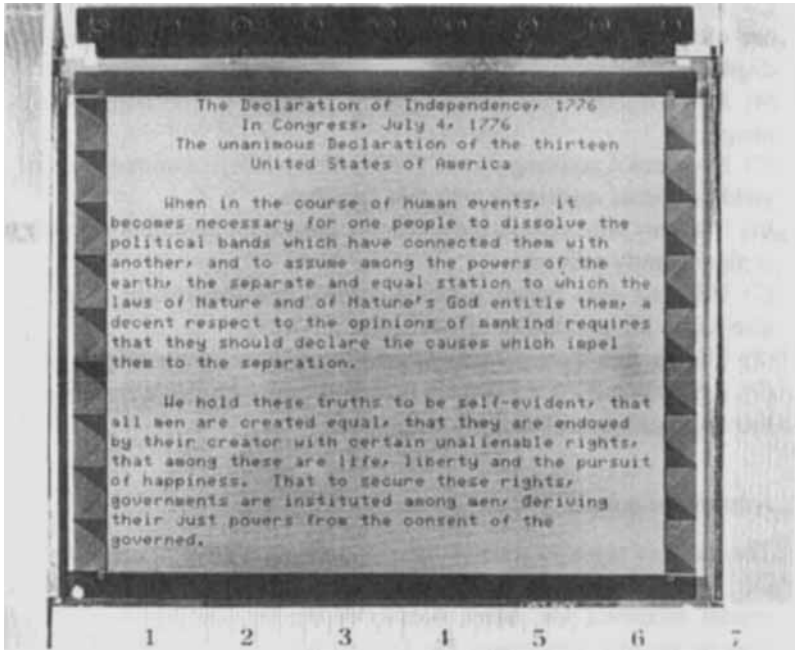

FIGURE 16 The 6″ × 7″, 288 × 360 dot matrix, 1200 character display.

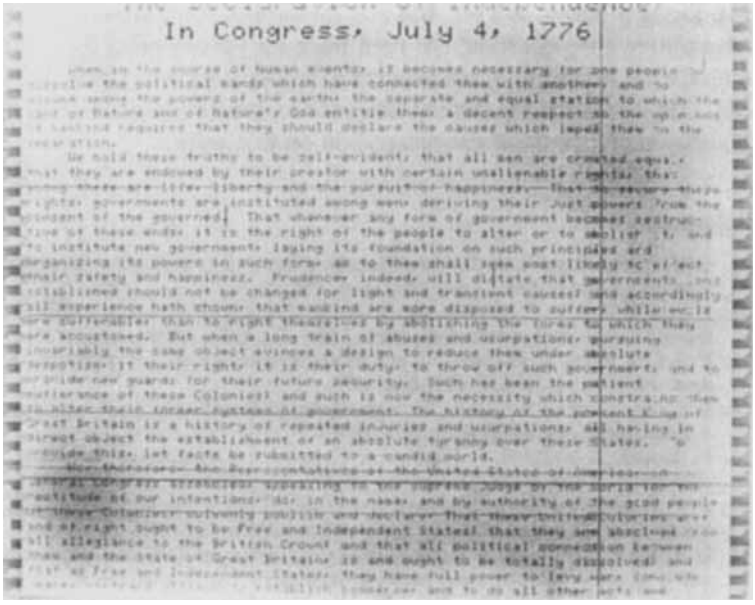

FIGURE 17 6″ × 7″, 512 × 576 matrix display fabricated with 3600 characters in 7 by 12 character format.

(3) The absence of polarizers which results in high brightness and removes one of the highest cost elements compared to twist nematic liquid crystal displays.
(4) Bright internal reflectors are possible, resulting in a crisp, nonparallax image.
(5) No internal assisting matrix (TFTs, diodes, etc.); avoiding the cost and yield problems associated with this approach.
(6) The very thin cell spacing constraint typical for high multiplexed LCDs is significantly relieved.
(7) Utilizing dyes makes possible colored and black/white displays and also raises the possibility of dual color devices.
(8) The devices have permanent memory, a novel and useful feature.
(9) All the non-TV CRT display functions can be implemented with proper thermal management design.

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References

1. G. H. Heilmeier and L. A. Zanoni, "Guest-host interactions in nematic liquid crystals. A new electro-optic effect," *Appl. Phys. Lett.*, **13**, 91–92, Aug. 1, 1968.
2. T. Uchida, H. Seki, C. Shishido, and M. Wada, "Guest-host interactions in nematic liquid crystals with twisted and tilted alignment," *Mol. Cryst. Liq. Cryst.*, **54**, 161–174, 1979.
3. H. S. Cole and R. A. Kashnow, "A new reflective dichroic liquid crystal display device," *Appl. Phys. Lett.*, **30**, 619–621, June 1977.
4. D. L. White and G. N. Taylor, "New absorptive mode reflective liquid crystal display," *J. Appl. Phys.*, **45**, 4718–4723, Nov. 1974.
5. K. Suzuki, T. Ishibashi, M. Satoh, and T. Isogai, "A multiplexed phase-change-type color LCD," *IEEE Trans. Elec. Dev.*, **28**, 719–723, 1981.
6. D. E. Castleberry, "Varistor controlled multiplexed liquid crystal display," Conference Record of 1978 Biennial Display Research Conference, Oct. 1978.
7. D. R. Baraff, J. R. Long, B. K. MacLaurin, C. J. Miner, and R. W. Streater, "The optimization of metal-insulator-metal nonlinear devices for use in multiplexed liquid crystal displays," *IEEE Trans. Elec. Dev.*, **28**, 736–739, 1981.

8. M. Hosokawa, K. Oguchi, M. Ikeda, S. Yazawa, and K. Endo, "Dichroic guest-host active matrix video display," 1981 Society of Information Display Symposium, Digest of Papers, 114–115, 1981.
9. W. A. Crossland and P. J. Ayliffe, "A dyed phase change liquid crystal display over a MOSFET switching array," 1981 Society of Information Display Symposium, Digest of Papers, 112–113, 1981.
10. M. Hareng, S. LeBerre, "Liquid crystal flat display," Int. Electron Devices Meeting, Tech. Digest, 258–259, Dec. 1978.
11. S. Lu, D. H. Davies, R. Albert, D. Chung, A. Hochbaum, and C. Chung, "Thermally addressed pleochroic dye switching liquid crystal display," 1982 Society of Information Display Symposium, Digest of Papers, 238–239, 1982.
12. P. E. Cladis and S. Torza, "Growth of a Smectic A from a bend nematic phase and the smectic light value," *Journal of Applied Physics*, **46**, Nov. 2, 1975.
13. F. J. Kahn, *Applied Physics Letter*, **22**, 111, 1973.